WHAT IS CLAIMED IS:

1. A method of determining when a frame of information comprised of one or more data buffers of information being transmitted in a network processor has completed transmission by a transmission system therein, comprising the steps of:

providing a plurality of buffer control blocks, each having space for control information to link one buffer to another for transmitting information in each data buffer,

each of said buffer control blocks having a last bit flag bit having a first position wherein an additional data buffer is to be chained to a previous data buffer and a second position wherein no additional data buffer is to be chained to a previous buffer; and

supplying the position of said last bit flag bit in each buffer control block to the transmission system of said network processor.

2. The invention as defined in claim 1 wherein the control blocks are in a free buffer control block queue when not in use in conjunction with a data buffer, and wherein said last bit flag bit is in said second position when in the free buffer control block queue.

3. The invention as defined in claim 2 wherein said last bit flag bit in each buffer control block is flipped to the first position when said control block buffer has written therein a starting and ending address for the next data buffer.

4. The invention as defined in claim 1 wherein all of the buffer control blocks that have been associated with the data buffer are returned to the free buffer control block queue when the last bit flag bit in the last buffer control block is in the second position.

5. The invention as defined in claim 1 wherein each buffer control block contains error correction code when the last bit flag bit is in the second position.

6. The invention as defined in claim 1 wherein each of said buffer control blocks contains a parity when the last bit flag bit is in the first position.

7. The invention as defined in claim 1 wherein each buffer control block includes the next buffer address when the last bit flag bit is in either the first position or the second position.

8. The invention as defined in claim 7 wherein said next buffer address corresponds to the address of the next buffer control block and the next data buffer.

9. The invention as defined in claim 2 wherein said buffer control blocks are chained in a given order when in the free buffer control block queue.

10. A plurality of buffer control blocks for use in controlling the transmission of buffers of data in a frame in a network processor, comprising:

each buffer control block having space for control information to link one buffer to another for transmitting information in each data buffer;

each of said buffer control blocks having a last bit flag bit having a first position wherein an additional data buffer is to be chained to a previous data buffer and a second position wherein no additional data buffer is to be chained to a previous buffer.

11. The invention as defined in claim 10 wherein the control blocks are in a free buffer control block queue when not in use in conjunction with a data buffer, and wherein said last bit flag bit is in said second position when in the free buffer control block queue.

12. The invention as defined in claim 11 wherein said last bit flag bit in each buffer control block is flipped to the first position when said control block buffer has written therein a starting and ending address for the next data buffer.

13. The invention as defined in claim 10 wherein each buffer control block contains error correction code when the last bit flag bit is in the second position.

14. The invention as defined in claim 10 wherein each of said buffer control blocks contains a parity when the last bit flag bit is in the first position.

15. The invention as defined in claim 10 wherein each buffer control block includes the next buffer address when the last bit flag bit is in either the first position or the second position.

16. The invention as defined in claim 15 wherein said next buffer address corresponds to the address of the next buffer control block and the next data buffer.

17. The invention as defined in claim 11 wherein said buffer control blocks are chained in a given order when in the free buffer control block queue.